Determine the effective address and the operand to be loaded for the following address modes:

(i) Direct

(ii) Immediate

(iii) Indirect

(iv) Relative

(v) Base register Addressing

(vi) Register indirect addressing (6)

(b) What is DMA? Briefly explain following terms with respect to DMA :

(i) Bus request

(ii) Bus Grant

(iii) Burst transfer

(iv) Cycle Stealing (5)

(c) What is cache memory? Mention its advantages and disadvantages. (4)

[This question paper contains 8 printed pages.]

Your Roll No.....

Sr. No. of Question Paper : 1584 **G**

Unique Paper Code : 2342011102

Name of the Paper : Computer System Architecture

Name of the Course : **B.Sc. (H) COMPUTER SCIENCE (NEP-UGCF-2022)**

Semester : I

Duration : 3 Hours Maximum Marks : 90

Instructions for Candidates

1. Write your Roll No. on the top immediately on receipt of this question paper.
2. Question No. **1** is compulsory.
3. Attempt **any 4** questions from Question **2** to Question **7**.
4. Parts of a question must be answered together.

1. (a) Perform the following conversions to the indicated bases : *(6)*

(i) $(973)_{10} = (?)_5$

(ii) $(F23A)_{16} = (?)_8$

(iii) $(10110.11)_2 = (?)_{10}$

(b) Give microinstructions for the following register reference instructions of the basic computer

(i) CMA

(ii) SPA (3)

(c) Simplify the following expression using Boolean algebra (3)

$$Y = (A+B)\ (A+C')\ (B'+C')$$

(d) Differentiate between microprogrammed and hardwired control unit. (3)

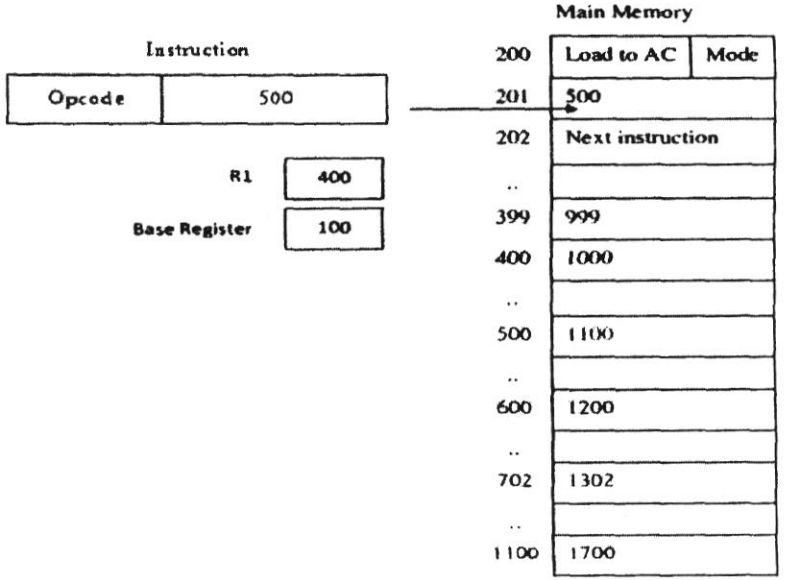
(e) Give Characteristic table and excitation table of SR flip-flop. (3)

(f) Construct a 16-to-1 line multiplexer with two 8-to-1 line multiplexers and one 2-to-1 line multiplexer. Give block diagram for the same. (3)

(g) Perform the arithmetic operation (–153) + (–250) using 10's complement. (3)

(c) Prove that X-OR is complement of X-NOR with the help of a truth table. (4)

7. (a) A two-word instruction to perform the load operation is stored in memory at an address 200 as represented in the memory map given below. The address field of the instruction is stored at address 201. The mode field specifies an addressing mode. R1 is the general-purpose register, which has the value of 400. Base register contains the value 100.



(ii) Draw the instruction word format. (5)

(c) Write down the difference between isolated I/O and memory mapped I/O. (4)

5. (a) Give the microinstructions of BSA instruction for the basic computer. Explain its working with the help of an example. How does it retrieve the return address. (6)

(b) Explain interrupt cycle with the help of a flowchart. (5)

(c) What is GPU? How is it different from CPU? (4)

6. (a) Design a combinational circuit that will indicate whether 4-bit number is either "odd and greater than 8" OR "even and less than 5". Assume 0 to be an even number. (6)

(b) (i) Construct a 6-to-64-line decoder using four 4-to-16-line decoders with enable input and one 2-to-4-line decoder.

(ii) Differentiate between RAM and ROM. (5)

(h) Why is Input Output Interface required between peripheral devices and CPU? (3)

(i) How many 256 × 8 ROM chips are needed to construct a memory of size 2048 × 8. Specify the number of address lines required for the newly constructed memory. (3)

2. (a) Given the Boolean function $F(A, B, C, D) = \Sigma(0, 5, 6, 7, 10, 13)$ and don't-care conditions $d(A, B, C, D) = \Sigma(1, 2, 3, 15)$ (6)

(i) Simplify Boolean expression F in SOP form using Karnaugh map.

(ii) Find complement of the simplified expression Fusing De-Morgan's Law.

(iii) Draw the logic diagram of the simplified expression F.

(b) Perform the arithmetic operation (–17) + (–27) in binary using signed 2's complement representation for negative numbers (Use 6-bit registers). Specify, if the operation results in overflow or not? (5)

(c) Describe the working of 4-bit binary adder subtractor circuit with the help of an example. (4)

3. (a) Draw a space-time diagram for a six-segment pipeline to process eight tasks. A non-pipelined system takes 50ns to process a task. The same task processed in six segment pipeline with a clock cycle of 20ns. Determine the speed up ratio of pipeline for 200 tasks. (6)

(b) What is the microprogrammed control unit? Write the microoperations that will be executed when the following 14-bit control word are applied :

(i) 010 001 110 00101

(ii) 101 001 111 01010

Given the binary code for ADD is 00101 and SUB is 01010 and three-bit binary code for selecting the register corresponds to the register number. (5)

(c) What is the difference between a direct and an indirect address instruction? How many references to memory are needed for such type of instruction to bring an operand into a processor register? (4)

4. (a) The content of PC in the basic computer is 2AC. The content of AC is 2EC3. The instruction format has three parts: mode (1-bit), opcode (3-bits), and

address part (12-bits). The content of memory at address 2AC is 832E. The content of memory at address 32E is 0821. The content of memory at address 821 is 8B9F (all numbers are in hexadecimal and 3- bit opcode 000 represents AND operation).

(i) Draw a block diagram of memory unit to give snapshot of the above representation and specify the instruction that will be executed.

(ii) Perform the binary operation in AC when the instruction is executed. Also, specify the values of PC, AR, DR, AC and IR in hexadecimal at the end of the instruction cycle. (6)

(b) A computer uses a memory unit with 65536 words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, address mode part to specify one of the four addressing modes, register code part to specify one of the 50 registers and an address part?

(i) How many bits are there in the operation code, addressing mode part, register code part, and address part?