SET-A

Unique Paper Code : 32341102

Name of the Course : B.Sc. (H) Computer Science

Semester : I

Duration : 3 Hours **Maximum Marks: 75**

Instructions for the Candidates

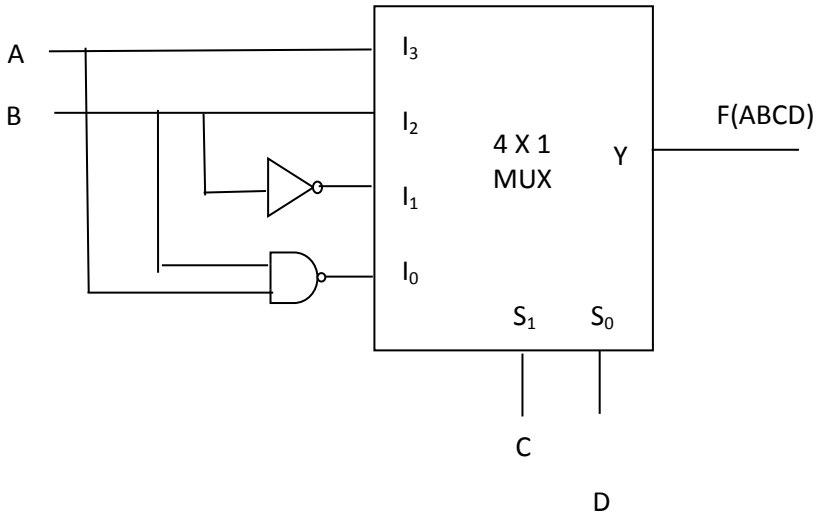
Attempt Any ***Four*** Questions. All Questions Carry Equal Marks

Q1.

- Given the Boolean function $\boldsymbol{F = xy + x(yz' + yz)}$
  - List the truth table of the function F.
  - Draw the logic diagram with NOR gates only.
  - Simplify the algebraic expression using Boolean algebra Rules.
  - Find complement of the optimized expression F using De-Morgan's Law.
- If $\boldsymbol{A'B + CD' = 0}$, then prove that:
  $\boldsymbol{AB + C'(A' + D') = AB + BD + (BD)' + A'C'D}$.
- Simplify the Boolean function $f(A, B, C, D) = \sum(0, 2, 4, 8, 10, 14)$ with don't care conditions $d(A, B, C, D) = \sum(6, 7, 12, 15)$ using Karnaugh map in
  - Sum-of-Products (SOP) form.
  - Product-of-Sums (POS) form.

Q2.

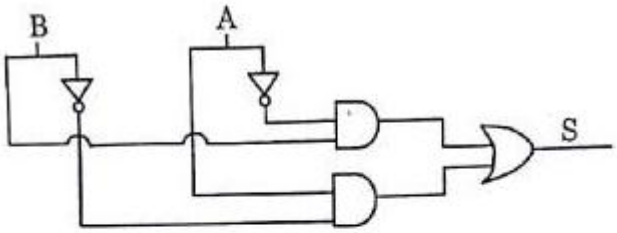
- What range of hex address values are used in $256K$ memory? To expand the $16K \times 8$ memory to a $256K \times 16$ organization, how many more $16K \times 8$ RAMs are required?
- What is the bit storage capacity of a ROM with 512×8 organizaion?
- Write the Boolean expression for the function F(ABCD) explained by logic circuit shown below.

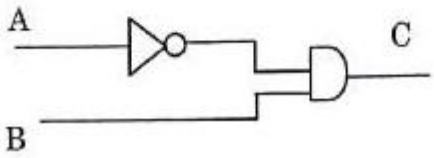


- Convert the hexadecimal number 5E7B2D.78 to its binary and octal

equivalent.

- Give decimal representation of $(A983)_{11}$.
- Add two BCD numbers 2856.25 and 1767.35.
- Subtract $(3655)_7$ from $(6146)_7$ using 8's complement.
- Give Boolean expression for outputs S and C in the logic circuit shown below (A and B are inputs).





Q3.

- Three 16-bit registers AC, DR, and TR, initially have the following values:

  AC 0011 1100 1111 1000

  DR 1100 1000 1001 0000

  TR 0011 0000 1000 1100

- The following sequence of micro-operation is performed sequentially on the registers. Indicate the value of the registers after each step.

$$AC \leftarrow AC + DR$$

$$DR \leftarrow TR$$

$$AC \leftarrow \overline{AC}$$

$$AC \leftarrow AC \ \wedge \ DR$$

- A Computer uses a memory unit with 32768 words of 48 bits each. Two instruction codes in binary are stored in one word of memory. The instruction has four parts: two bits to specify mode, two bits to specify a processor register, an operation code, and an address part.
  - Draw the instruction word format and indicate the number of bits in each part.
  - How many addressing modes and number of operations are supported?
  - Specify the number of bits required in each of PC, AC and IR.
- Explain why these micro-operations cannot execute in single clock pulse.

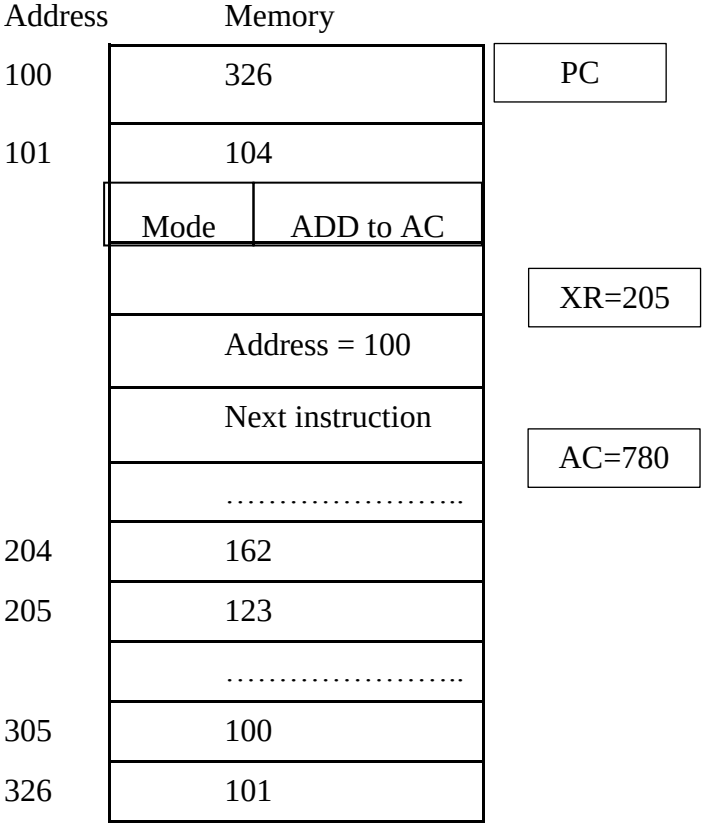
Rewrite the following micro-operations so that they can be executed in single clock pulse.

- $M[PC] \leftarrow AR, PC \leftarrow AR + 1$
- $AC \leftarrow M[AR], SC \leftarrow 0$
- $TR \leftarrow AC \wedge DR, E \leftarrow C_{out}$

Q4.

- Write a program using one address instructions to evaluate the arithmetic expression $X = (A * B + C)/(D - E)$.

- Consider the following snapshot of memory to answer the following questions.



  - A two-word instruction "ADD to AC" being currently executed is stored at location 102 with its address field at location 103. The Accumulator register AC receives the result after the instruction is executed. (All numbers are in decimal). Evaluate the effective address and value of AC after the execution of this instruction if the addressing mode of the instruction is:
    - Direct
    - Immediate
    - Indirect
    - Relative
    - Indexed addressing mode with XR as the index register.

- According to general register organization of a computer, an 18-bit binary control word consists of three fields SELA, SELB, SELD for selecting 16 registers each and operation OPR. Specify the control word that must be applied to the processor to implement the following microoperations using Table 1.

  - $R2 \leftarrow R2 + R3$
  - $R7 \leftarrow R9 \wedge R7$
  - $R5 \leftarrow shr\ R5$
  - $R1 \leftarrow 0$

Table 1. Encoding of ALU operations

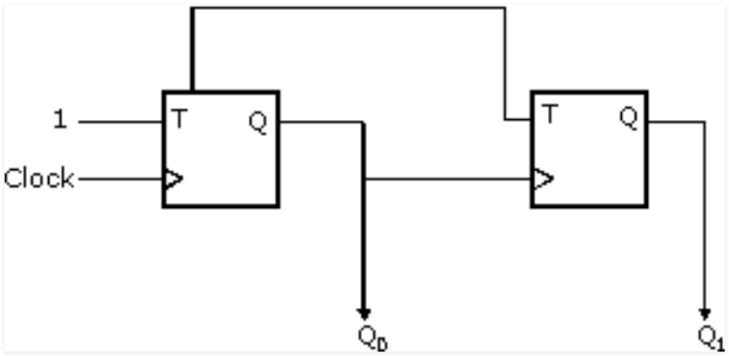
OPR Select	**Operation**
010001	ADD
001100	AND
010000	SHRA
111100	XOR

Q5.

- Give the sequence of microinstructions needed to perform memory reference instruction in the basic computer which
  - branches to the address specified if value of AC is greater than DR.
  - performs shift left operation to the value of AC.
  - performs OR operation between the value of AC and DR.
  - performs shift right operation to the value of AC.
- Consider X and Y as a synchronous pipeline processor. Design X has six segments with execution time of 7ns, 5ns, 3ns, 4ns, 2ns and 1ns. Design Y has nine segments each with 3 ns execution time. Compare the performance of both designs for executing 100 tasks.
- Give the excitation table for a flip flop AB whose characteristic table is given as follows:

A	**B**	**Q(t+1)**
0	0	Q'(t)
0	1	1
1	0	0
1	1	Q(t)

- In the sequential circuit shown below, if the initial value of the output Q_0Q_1 is 01, what are the next four values of Q_0Q_1 ?



Q6.

- Explain the conditions for the bidirectional controller line of DMA to be used as inputs and outputs.
- Suppose that DMA controller transfers 32-bit words to memory using cycle stealing. It transmits character at rate of 4800 character per second. Whereas, the CPU fetches and executes an instruction with average rate 1 million instruction per second. How much CPU will be slow down due to DMA transfer?
- A system uses DMA for data transfer from a magnetic disk to memory to transfer 512 words to a memory section starting from address 1024. Give the initial values that the CPU must transfer to the DMA controller to initiate this transfer.
- Consider a hypothetical computer which has five interrupt requests during data transfer between CPU and I/O device. Write the procedure that machine can establish interrupts in interrupt service routine. Explain how the interrupt service routine will be executed without priority interrupt hardware.