(*b*) Evaluate (+80) + (+90) and (–80) + (–90) with binary numbers in signed-2's complement representation. Use eight bits to accommodate each number together with its sign. 3+3=6

3. (*a*) What is an interrupt cycle ? Draw a flowchart depicting the interrupt cycle. 5

(*b*) What is addressing mode ? An instruction is stored at location 500 with its address field at location 501. The address field has the value 600. The content of a processor register R1 is 300. Evaluate the effective address (EA) if the addressing mode of the instruction is : 5

(*i*) Direct

(*ii*) Relative

(*iii*) Immediate.

13/12/18 (M)

This question paper contains **4+2** printed pages]

Roll No. | | | | | | | | | | |

S. No. of Question Paper : **47**

Unique Paper Code : **32341102** **I**

Name of the Paper : **Computer System Architecture**

Name of the Course : **B.Sc. (H) Computer Science**

Semester : **I**

Duration : **3 Hours** Maximum Marks : **75**

(Write your Roll No. on the top immediately on receipt of this question paper.)

Question No. **1** is compulsory.

Attempt any **4** questions out of Question Nos. **2** to **7**.

Parts of a question must be answered together.

1. (*a*) Convert the following numbers with the indicated bases to decimal : 2

(*i*) $(121121)_3$

(*ii*) $(4310)_5$.

(*b*) Given the Boolean expression $F = x'y + xyz'$, show that $F.F' = 0$. 2

P.T.O.

(*c*) Draw a block diagram and function table of 4-to-1 line multiplexer. 2+2=4

(*d*) Simplify the following Boolean function using a three-variable Karnaugh map : 4

$$F(x, y, z) = \Sigma(1, 2, 3, 6, 7).$$

(*e*) Differentiate between a direct and an indirect address instruction. How many references to memory are needed for each type of instruction to bring an operand into a processor register ? 2+2=4

(*f*) Explain the purpose of Auto-increment and Auto-decrement addressing modes. 2

(*g*) Write *two* instructions needed in the basic computer in order to set the extended bit E to 1. 2

(*h*) Specify the 14-bit binary control word that must be specified to the processor in terms of SELA, SELB, SELD and OPR to implement the following micro-operation :

$$R1 \leftarrow R2 - R3.$$

Where the binary code for OPR is 00101, and the three bit binary code for the selecting the register corresponds to the register number. 2

(*i*) Determine the number of clock cycles that it takes to process 150 tasks in a six-segment pipeline. 2

(*j*) List *three* uses of an I/O processor. 3

(*k*) What is Content Addressable Memory (CAM) ? Explain its hardware organization with the help of a block diagram. 1+3=4

(*l*) Write micro-operations for implementing the following memory reference instructions : 2+2=4

(*i*) BUN

(*ii*) STA.

2. (*a*) Explain why each of the following register transfer language statements cannot be directly executed in a basic computer. Also specify the right sequence of micro-operations that will be required to perform these operations : 2+2=4

(*i*) $IR \leftarrow M[PC]$

(*ii*) $AC \leftarrow AC + TR$.

7. (*a*) Design full adder and derive the Boolean expressions for sum and carry outputs of the full adder. 6

(*b*) A computer uses a memory unit with 1024K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has 4 parts : an indirect bit, an operation code, a register code part to specify one of 128 registers and an address part : 4

(*i*) How many bits are there in the data and address lines ?

(*ii*) Draw the instruction word format and compute the number of bits required for each part.

4. (*a*) Explain the function of the following registers in a basic computer : 5

(*i*) PC

(*ii*) AR

(*iii*) IR

(*iv*) AC

(*v*) DR.

(*b*) Show the step-by-step process of multiplying two binary numbers using Booth's Algorithm. Assume multiplicand = 01111 and multiplier = 10011. 5

5. (*a*) Draw the block diagram of a Direct Memory Access (DMA) controller and explain its working. 3+3=6

(*b*) Convert $(215)_{10}$ to : 2+2=4

(*i*) 12-bit Binary Coded Octal

(*ii*) 12-bit Binary Coded Hexadecimal.

6. (*a*) Draw a space-time diagram for a four-segment pipeline showing the time it takes to process six tasks. 4+1=5

(*b*) Draw the flowchart for programmed I/O mode of data transfer and explain its working. 2+3=5